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Clock Gating Cells for Low Power Scan Testing By Dft Technique

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ABSTRACT
This paper presents about minimizing the power consumption by scan testing DFT technique. In Integrated Circuit technology entire thing depends on floor plan, Power consumption, Timing, and routing. Present days we improved a lot in all sectors except power consumption to improve the speed of device the clock toggle rate plays a key role due to that power drop is also more. So in IC technology the unused clock signal are present in sequential circuits when the data path or data signal arrived late .So in order to know the unused clock signals we used scan based testing through DFT. After testing that the unused or unwanted clock signals can avoiding temporarily by placing the clock gating cells by that it decreases and high controllability leads to avoid heating and power consumption problems.
Keywords: DFT, clock gating, toggle rate, power consumption.

I. INTRODUCTION

In recent years structural (mostly scan-based) tests have come to be the dominant mechanism for volume IC manufacturing. At _rst, low-speed scan tests measured against the stuck-at coverage metric were considered adequate. But, in recent technologies, at-speed test has become a requirement in order to maintain su_cient levels of outgoing quality . Adding at-speed structural tests to the standard suite of production tests presents an array of new problems. What are the design for test (DFT) requirements that must be met in order to be able to generate high quality at-speed scan tests? What are the tester limitations that must be comprehended? If low cost testers are to be used, what additional constraints do they place on the problem? Many of the practical issues associated with structural at-speed tests were addressed by the authors and others in recent publications [7]. One of these new problems is associated with switching power consumption during test. It is well known that power consumption during the test mode of operation can exceed that during normal functional or \mission mode" operation . This fact is true even for relatively slow speed scan operation. In the case of structural at-speed testing such as for transition or path delay faults, power consumption is a concern not only from the standpoint of scan shifting but also for the high speed capture operation. Very high power demands during test can cause unnecessary yield loss as well as exacerbate already troublesome issues associated with IR-drop and crosstalk [8]. Excessive power consumption can also induce unacceptably high stress-related failures. Excessive switching power consumption during test can be tackled in multiple ways. Test patterns can be generated to reduce switching activity while possibly increasing pattern volume [8]. Power grid design can be made to comprehend increased test power demands. Logical DFT techniques can be devised to reduce power; these typically involve clock gating or design partitioning. A prior publication gives a longer list of references in this area [15]. In this paper, we will begin by presenting pattern generation approaches to minimize power consumption that would be used if power-related problems were discovered after design completion. We investigate various heuristics for modifying test content to address power concerns. These techniques require no modi_cations to the basic design nor its test logic. We compare the heuristics in terms of the amount of switching reduction, and also the increase in pattern volume and decrease in coverage for a given fault coverage _gure of merit. The minimum transition fill is also deployed in [33] to reassign new values to unspecified positions whose locations are determined by bit-stripping indicating whether turning a bit into unspecified one will affect fault coverage. If so, then the bit is returned to its original value, otherwise it is kept as a don't care. Other forms of filling are aimed at decreasing capture power dissipation. They are guided by rules of suitability, which provide values that should be assigned to unspecified bits so that the number of transitions at the outputs of scan cells in the capture mode is minimized. Other techniques proposed to address the low capture power include [21] and Low power test data encoding schemes adopt conventional LFSR reseeding techniques to reduce the scan-in transition probability. In particular, the method of uses two LFSRs to produce actual test cubes and the corresponding mask bits. Outputs of both LFSRs are AND-ed or OR-ed to

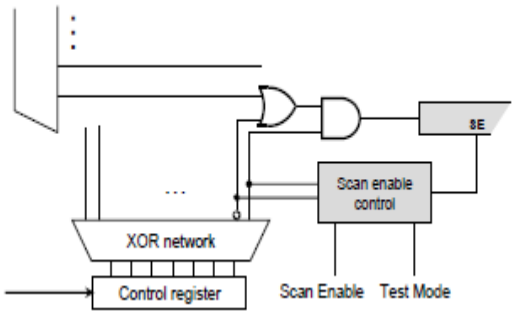
decrease the amount of switching. The use of extra seeds may compromise compression ratios, and therefore the scheme of [22] divides test cubes into blocks and only uses reseeding to encode blocks that contain transitions. Other blocks are replaced with a constant value which is fed directly into scan chains. Some of the above schemes such as design partitioning and scheduling can reduce global power during both shift and capture. Even if they are employed, power reduction is often still necessary for the design partitions being tested in a given session. Thus, a method is required that is nonintrusive to the design and design flow; can control power during scan loading, unloading, and capture; and supports embedded compression with high compression ratios.

II. II POWER CONSUMPTION DURING TEST

In order to analyze power consumption during test, it is best to break test operation into its twoDuring scan capture, especially at high speed, new problems become apparent. IR-drop and crosstalk effects which would normally not be observed at low speed suddenly materialize [8]. Also, due to the high demands on the clock tree during the high speed captures, unintentional wave shaping and cycle stretching may occur on the clock pulses, with the net effect of either slowing the effective clock frequency [22] or suppressing the clock pulse(s) entirely. To solve this latter problem, it is possible to introduce clock gating to minimize the amount of logic switching during the capture cycle. However, doing so complicates timing closure and is thus undesirable. Just as in the case of scan shift, pattern content can be modified in such a way as to minimize simultaneous switching, and thus power consumption, during scan capture events. Previous work by the authors in investigating IR-drop and crosstalk showed that if most of the scan-in data were made the same, e.g., all 0's or all 1's, but particularly all 0's, then the post-capture data is often similar, thus suggesting that switching activity had been reduced. Power simulations performed in the authors' earlier work corroborated this hypothesis. This procedure has been referred to by others as \pattern scrubbing" [23] and similar ideas have appeared in earlier work [16]{[18]. Depending on the exact procedure used, reductions occur during scan shift as well as scan capture. The difficulty lies in identifying which bits to modify, and doing it while minimizing any other effects. It is risky, however, to assume that modifying pattern content will be an adequate solution in every case. It could be such that power consumption is so high that pattern modifications will be excessive and thus pattern volume high as well. Or, it could be that there is a great deal of variation in the amount of bits to be modified across the span of patterns in the test set, which will be discussed in the following section. In such cases, it is better to estimate power early in the design cycle, and plan and implement a design for test approach that maintains an acceptable level of switching activity while minimizing overall design impact. We will discuss such an approach later in this paper.

III. Scan shift-in operations

The combinational part of the control block is designed as an *m*-input *n*-output XOR mapping circuit, where *m* is the number of control bits, and *n* is the number of scan chains. In other words, each output of the block is obtained by XOR-ing certain control bits. The XOR network is configured in such a way that it guarantees high encoding efficiency, i.e., a close to 100% ratio of successfully encoded pre-specified gating signals to the number of control bits. The control circuitry operates as follows. For all scan chains having specified bits, the corresponding gating signals should be chosen in such a way that the AND gate have 1 on its input. Consequently, these scan chains can be driven directly from the decompressor. This process continues until pre-specified power limits are reached. As for the remaining scan chains, one can determine, using the XOR network and the control bits found earlier, those gating signals that were not encoded. The gating circuitry of Fig. 3 allows the decompressor to drive approximately 50% of such scan chains, while the remaining ones receive a constant 0. Indeed, a single output of the XOR network is producing 0 with probability 0.5 (except rare cases when the number of asserted control variables is very small), and thus the gating signal reaches the AND gate and then a scan chain as a constant 0. Note that several experimental results [5] indicate lower switching activity when the scan chains are loaded with the constant 0 rather than the constant 1. Even if this is circuit-specific feature, it nevertheless appears to be the case across several designs. *Two constant stimuli*. In certain applications it might be desirable or convenient to feed scan chains with both logic values of 0 and 1 acting as constant stimuli. Consider scan chains that were not the subject of encoding, as discussed in the previous paragraph. The gating circuitry shown in Fig. 4 allows the decompressor to drive approximately 25% of such scan chains, while 50% of them receive a constant 0, and 25% have a constant 1. In other words, roughly 75% of scan chains with no specified bits will have no transitions at all. Indeed, as shown earlier, a gating signal reaches the AND gate and then a scan chain as a constant 0 with probability 0.5. On the other hand, in order to get a constant 1, two gating signals are needed - one set to 0 and driving the OR gate, and the other one set to 1 and feeding the AND gate. Clearly, the XOR network outputs this combination with probability 0.25.



The fraction of scan chains driven by the decompressor can be changed in the manner of Fig. 5 by adding a *biasing circuitry*, i.e., the group of AND gates driven by the XOR network. With these gates in place, the decompressor is capable of driving approximately 25% of scan chains. This percentage can be reduced even further by adding more inputs to the AND gates. For example, the third input reduces the percentage of scan chains driven by the decompressor down to 12.5%, while the fraction of scan chains getting the constant value of 0 increases accordingly, as shown earlier. *Reduction of control data volume*. When generating test patterns, it is possible to make different test patterns sharing the same control data such that the control data can be loaded into the programmable controller only once for multiple test patterns and only the unique control data is stored in the external tester. To maximize the control data to be shared with different test patterns, the ATPG can be enhanced to prefer the control data that meets current requirement and is used by the test patterns generated before when there are multiple choices.

IV. Conclusions

In this paper, we propose a comprehensive scan test application scheme encompassing efficient techniques to reduce power dissipation in the continuous flow EDT environment during scan loading, unloading, and capture. Experimental results confirm that for industrial designs, our scheme results in substantial reduction of test power. Switching activity during scan loading and unloading is reduced by up to 96% (24x) and 87% (8x), respectively, using the proposed low-power decompressor. Average switching during capture is reduced by up to 70% using a combination of low-power decompressor and clock gater control. Using only clock-gater control, switching is reduced by up to 57%. The peak capture switching is reduced by up to 32%. Such significant power reductions create a margin that allows accelerating scan shifting which, in turn, effectively decreases test application time. It also enables more of the design to be tested in a given session, enabling a reduction in test time as well. The same methodology allows one to operate within specified power consumption budgets without compromising test quality. Finally, the presented approach fits into the core-based design paradigm, and complements design partitioning schemes for power reduction.

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